**ECE 586 Spring 24**

**ROLES & RESPONSIBILITIES:**

We as in Sai Tagore, Surya Vamsi, Divya Sri & Rafath have worked with a great co-ordination to complete this MIPS Lite Architecture Project, coming to roles and responsibilities, we have divided our work equally among ourselves to complete the project as soon as possible without any errors and without any miss conceptions.

1. **Suggu Tagore -** Gathered all the details and learnt and executed the instruction Decode and

Execute stage related operations and worked on the code and created a pseudo code and

documented the data related to instruction decode and execute stage, equally contributed in

testbench top creation and documentation.

2. **Divya Sri Ayluri –** Gathered all the details and learnt and executed the instruction fetch

stage operations and worked on the code and created a pseudo code and documented the data

related to instruction fetch. equally contributed in testbench top creation and documentation.

3. **Rafath Achugatla –** Gathered all the details and learnt and executed the Memory stage related

operations and worked on the code and created a pseudo code and documented the data

related to instruction memory stage. equally contributed in testbench top creation and

documentation.

4. **Surya Vamsi -** Gathered all the details and learnt and executed writeback stage in the

pipeline related operations and worked on the code and created a pseudo code and

documented the data related to write backstage. equally contributed in testbench top creation

and documentation.